Aangeboden projecten: Details project

Improving quantum circuit extraction for ZX-diagrams (John van de Wetering)
Master Logic
4 Nov 2022

1.1 Proposal
Thesis project proposal

1.2 Project Title
Improving quantum circuit extraction for ZX-diagrams

1.3 Project Description

The ZX-calculus is a graphical language for reasoning about quantum computing in a direct way, working directly with diagrams instead of the underlying matrices. They are more general than the unitary quantum circuits that can actually be run on a quantum computer. As such we need to sometimes find a way to translate a ZX-diagram back into a quantum circuit. This problem is known as 'circuit extraction' and is generally known to be hard. There are however certain regimes where we know how to do it. If you choose this as your thesis topic, there are a variety of ways we can take this project:
Expanding circuit extraction from unitary diagrams to isometries and states. This is useful when we know which state we want to input into a quantum computation, and allows us to do more optimisation.
Figure out ways to do circuit extraction where we allow for a limited amount of post-selection (this is when we do a measurement and only continue when we get a certain desired outcome). This might be useful for near-term quantum computers where we can quickly do many samples and throw away those that are undesirable. Using such techniques we could extract a larger set of diagrams which we can't extract into non-post-selected circuits right now.
We know that general circuit extraction (without any further promises) is at least #P-hard. We however only have a very rough upper bound on the complexity. It might be possible to establish the exact complexity upper bound.

Prerequisites: Knowledge about quantum computing woul be useful (like Ronald de Wolff's Mastermath course), but is not necessary. The student must have strong mathematical skills. The interested student can read the following papers for more background:
General ZX-calculus review: https://arxiv.org/abs/2012.13966
Explainer about circuit extraction: https://arxiv.org/abs/2003.01664
Proof of hardness of circuit extraction: https://arxiv.org/abs/2202.09194

1.4 Work environment

The student will meet regularly with the supervisor. Pending available space, the student will be given an office to work from.

1.5 Expectations

Perform research, possibly write code, and finish the project with writing a thesis.

Duration

- MSc Information Studies and MSc Logic: 6 months

- MSc Software Engineering: 3 months

- MSc Computational Science: 8 months

1.10 Programmes
Master Logic (6 months)

1.11 Project Contact
John van de Wetering (j.m.m.vandewetering@uva.nl, IVI)

1.12 Number of Students
1

2. Research Tags

Please choose a maximum of three individual tags.
Note: it is not possible to submit the form if more than 3 research tags are selected

2.1 Amsterdam Machine Learning Lab

2.2 Computational Science Lab

2.3 Computer Vision

2.4 Digital Interactions Lab

2.5 Intelligent Data Engineering Lab

2.6 Information Retrieval Lab

2.7 Language Technology Lab

2.8 Multimedia Analytics Lab Amsterdam

2.9 Quantitative Healthcare Analysis

2.10 Theory of Computer Science Quantum computing

2.11 Complex Cyber Infrastructure

2.12 Security by Design

2.13 Multiscale Networked Systems

2.14 Parallel Computing Systems

2.15 Socially Intelligent Artificial Systems

2.16 Video and Image Sense Lab

2.17 Natural Language Processing & Digital Humanities

2.18 Theoretical Computer Science (ILLC)

2.19 Formal Semantics and Philosophical Logic

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